Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (1/98)
Approved for use through 09/30/2000 OMB 0651-0032
Patent and Trademark Office U S DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No. 0756-2222

First Inventor or Application Identifier: Shunpei YAMAZAKI et al.

Title. METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE

Express Mail Label No.

JC917 U.S. PTO 09/699466 10/31/00

JC803 U.S. PTO 10/31/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

1. [X] Fee Transmittal Form (e g , PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [49]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [7]
4. [X] Oath or Declaration *Total Pages* [3]
   a [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1 63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1 33(b)
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

6 [ ] Microfiche Computer Program *(Appendix)*

7 Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a [ ] Computer Readable Copy
b [ ] Paper Copy (identical to computer copy)
c [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8 [ ] Assignment Papers (cover sheet & document(s))
9 [ ] 37 CFR 3 73(b) Statement [ ] Power of Attorney
(when there is an assignee)
10 [ ] English Translation Document *(if applicable)*
11 [X] Information Disclosure Statement [ ] Copies of IDS Citations
(IDS)/PTO-1449
12 [X] Preliminary Amendment
13 [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14 [ ] *Small Entity [ ] Statement filed in prior application, Status still proper and desired
Statement(s)
(PTO/SB/09-12)
15 [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16 [X] Other Notice of Change of Company Name and Address

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment*
Divisional of prior application Serial No. 08/784,290, filed January 16, 1997
Prior application information: Examiner: B. Dutton Group/Art Unit: 2823

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label Customer No 22204 or [X] Correspondence address below

(Insert Customer No or Attach bar code label here)

Name Jeffrey L Costellia
Firm. NIXON PEABODY LLP
Address 8180 Greensboro Drive, Suite 800
City McLean State VA Zip Code 22102
Country. U S.A. Telephone (703) 790-9110 FAX (703) 883-0370

Name: Eric J. Robinson Registration No. 38,285

Signature Date: October 31, 2000

Burden Hour Statement This form is estimated to take 0.2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO. Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

PTO/SB/17 (1/98)
Approved for use through 09/30/2000 OMB 0651-0032
Patent and Trademark Office U S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1 These are the fees effective October 1, 1997 Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid See Forms PTO/SB/09-12

TOTAL AMOUNT OF PAYMENT $1,040 00

Complete If Known	
Application Number	
Filing Date	October 31, 2000
First Named Inventor	Shunpei YAMAZAKI et al
Examiner Name	B Dutton
Group Art Unit	2823
Attorney Docket Number	0756-2222

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to·
Deposit Account No 19-2380
Deposit Account Name NIXON PEABODY LLP

[X] Charge Any Additional Fee Required Under 37 CFR 1 16 and 1.17
[ ] Charge the Issue Fee Set in 37 CFR 1 18 at the Mailing of the Notice of Allowance

2. [X] Payment Enclosed·
[X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	[710]
106	320	206	160	Design filing fee	[ ]
107	490	207	245	Plant filing fee	[ ]
108	710	208	355	Reissue filing fee	[ ]
114	150	214	75	Provisional filing fee	[ ]

SUBTOTAL (1) $710 00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from Below	Fee Paid
Total Claims	25	- 20** =	5	X $18 00 = $ 90.00
Independent Claims	6	- 3** =	3	X $80 00 = $240.00
Multiple Dependent Claims				$270.00 = $

**or number previously paid, if greater, For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $330.00

FEE CALCULATION (continued)

3 ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge-late filing fee or oath	
127	50	227	25	Surcharge-late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Ext for reply within first month	
116	380	216	190	Ext for reply within second mth	
117	870	217	435	Ext for reply within third mth	
118	1,360	218	680	Ext for reply within fourth mth	
128	1,850	228	925	Ext for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing brief in support of appeal	
121	260	221	130	Request for Oral Hearing	
138	1,510	138	1,510	Petition to institute public use proceeding	
140	110	240	55	Petition to revive-unavoidable	
141	1,210	241	605	Petition to revive-unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of IDS	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	760	246	380	Filing a submission after final rejection (37 CFR 1 129(a))	
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	
				Other	
				Other	

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) $

SUBMITTED BY

Complete (if applicable)

Typed or Printed Name	Eric J. Robinson			Reg. Number	38,285
Signature		Date	October 31, 2000	Deposit Account User ID	19-2380

Burden Hour Statement· This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Washington, DC 20231.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)
Shunpei YAMAZAKI et al.	)
Based On Serial No. 08/784,290	) Art Unit: 2823
Which Was Filed: January 16, 1997	) Examiner: B. Dutton
For: METHOD FOR FABRICATING	)
A SEMICONDUCTOR DEVICE	) Date: October 31, 2000

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of Application Serial No. 08/784,290, filed January 16, 1997.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

Method for Fabricating A Semiconductor Device

Field of the Invention

The present invention relates to a semiconductor device typified by a thin film transistor and to a fabrication method thereof. Specifically, the present invention relates to a semiconductor device using a crystalline silicon thin film formed on a glass substrate or a quartz substrate and to a fabrication method thereof.

Description of Related Art

Hitherto, there has been known a thin film transistor using a silicon film, i.e. a technology for forming the thin film transistor by using the silicon film formed on a glass substrate or quartz substrate.

The glass substrate or quartz substrate is used because the thin film transistor is used for an active matrix type liquid crystal display. While a thin film transistor has been formed by using an amorphous silicon film in the past, it is being tried to fabricate the thin film transistor by utilizing a silicon film having a crystallinity (referred to as "crystalline silicon film" hereinbelow) in order to enhance its performance.

The thin film transistor using the crystalline silicon film can operate at high speed by more than two digits as compared to one using an amorphous silicon film. Therefore, while peripheral driver circuits of an active matrix liquid crystal display have been composed of external IC circuits, they may be built on the glass substrate or quartz

substrate similarly to the active matrix circuit.

Such structure is very advantageous in miniaturizing the whole apparatus and in simplifying the fabrication process, thus leading to reduction of the fabrication cost.

In general, a crystalline silicon film has been obtained by forming an amorphous silicon film by means of plasma CVD or low pressure thermal CVD and then by crystallizing it by performing a heat treatment or by irradiating laser light.

However, it has been difficult to obtain a required crystallinity across the wide area through the heat treatment because it may cause nonuniformity in the crystallization.

Further, although it is possible to obtain the high crystallinity partly by irradiating laser light, it is difficult to obtain a good annealing effect across the wide area. In particular, the irradiation of the laser light is apt to become unstable under the conditions needed for obtaining the good crystallinity.

Meanwhile, a technology described in Japanese Patent Laid-Open No. Hei. 6-232059 has been known. This technology obtains a crystalline silicon film through a heat treatment at a lower temperature than that of the prior art by introducing a metal element (e.g. nickel) which promotes the crystallization of silicon to the amorphous silicon film.

This technology allows high crystallinity to be obtained uniformly across a wide area as compared to the prior art crystallization method by way of only heating or crystallization of an amorphous silicon film only by means of irradiation of laser light.

However, it is difficult to obtain a crystalline silicon film having high crystallinity and homogeneity across a wide area which is required for an active matrix type liquid

crystal display.

Further, because the metal element is contained within the film and an amount thereof to be introduced has to be controlled very carefully, there is a problem in its reproducibility and stability (electrical stability of a device obtained).

Still more, there is a problem that an elapsed change of the characteristics of a semiconductor device to be obtained is large or an OFF value, in case of a thin film transistor, is large, due to the influence of the remaining metal element.

That is, although the metal element which promotes the crystallization of silicon plays the useful role in obtaining the crystalline silicon film, its existence becomes a negative factor which causes various problems after obtaining the crystalline silicon film once.

Summary of the Invention

It is an object of the invention disclosed in the present specification to provide a semiconductor device having excellent characteristics by using a crystalline silicon film having a high crystallinity.

It is an object of the invention disclosed in the present specification to provide a technology for reducing concentration of a metal element within a crystalline silicon film obtained by utilizing the metal element which promotes crystallization of silicon.

It is another object of the present invention to provide a technology which can enhance characteristics and reliability of the semiconductor device thus obtained.

One of the inventions disclosed in the present specification is characterized in that it comprises steps of intentionally introducing a metal element which promotes crystallization of silicon to an amorphous silicon film and crystallizing the amorphous silicon film by a first heat treatment to obtain a crystalline silicon film; irradiating laser light or intense light to the crystalline silicon film; removing or reducing the metal element existing within the crystalline silicon film by performing a second heat treatment within an oxidizing atmosphere containing a halogen element; removing a thermal oxide film formed in the previous step; and forming another thermal oxide film on the surface of the region from which the thermal oxide film has been removed by performing another thermal oxidation.

An arrangement of another invention is characterized in that it comprises steps of intentionally introducing a metal element which promotes crystallization of silicon to an amorphous silicon film and crystallizing the amorphous silicon film by a first heat treatment to obtain a crystalline silicon film; irradiating laser light or intense light to the crystalline silicon film to diffuse the metal element, existing within the crystalline silicon film, in the crystalline silicon film; performing a second heat treatment within an oxidizing atmosphere containing a halogen element to cause the metal element existing within the crystalline silicon film to be gettered to a thermal oxide film to be formed; removing the thermal oxide film formed in the previous step; and forming another thermal oxide film on the surface of the region from which the thermal oxide film has been removed by performing another thermal oxidation.

An arrangement of another invention is characterized in that it comprises steps of intentionally introducing a metal element which promotes crystallization of silicon to an amorphous silicon film and crystallizing the amorphous silicon film by a first heat treatment to obtain a crystalline silicon film; forming an active layer of the semiconductor device by patterning the crystalline silicon film; irradiating laser light or intense light to the active layer; performing a second heat treatment within an oxidizing atmosphere containing a halogen element to remove or reduce the metal element existing within the active layer; removing a thermal oxide film formed in the previous step; and forming another thermal oxide film on the surface of the active layer by performing another thermal oxidation.

An arrangement of another invention is characterized in that it comprises steps of intentionally and selectively introducing a metal element which promotes crystallization of silicon to an amorphous silicon film; performing a first heat treatment to the amorphous silicon film to grow crystal in a direction parallel to the film from a region of the amorphous silicon film into which the metal element has been intentionally and selectively introduced; irradiating laser light or intense light to diffuse the metal element existing within the region where the crystal has grown; performing a second heat treatment within an oxidizing atmosphere containing a halogen element to cause the metal element existing within the region where the crystal has grown to be gettered to a thermal oxide film to be formed; removing the thermal oxide film formed in the previous step; and forming another thermal oxide film on the surface of the region from which the

thermal oxide film has been removed by performing another thermal oxidation.

An arrangement of another invention is characterized in that it comprises steps of intentionally introducing a metal element which promotes crystallization of silicon to an amorphous silicon film and crystallizing the amorphous silicon film by a first heat treatment to obtain a crystalline silicon film; forming an active layer of the semiconductor device by patterning the crystalline silicon film; irradiating laser light or intense light to the active layer; performing a second heat treatment within an oxidizing atmosphere containing a halogen element to remove or reduce the metal element existing within the active layer; removing a thermal oxide film formed in the previous step; and forming another thermal oxide film on the surface of the active layer by performing another thermal oxidation, wherein the active layer has a tapered shape in which an angle formed between a side face and an underlying face is 20° to 50°.

In the invention disclosed in the present specification, one or a plurality elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au may be used as the metal element which promotes the crystallization of silicon.

Further, as the oxidizing atmosphere containing the halogen element, an atmosphere to which one or a plurality of gases selected from HCl, HF, HBr, Cl_2, F_2 or Br_2 is added into an O_2 atmosphere or an atmosphere containing O_2 may be used.

The concentration of impurity in the present specification is defined as the minimum value of measured values measured by the SIMS (secondary ion mass spectrometry).

According to a preferred mode for carrying out the invention disclosed in the present specification, an amorphous silicon film is formed at first. Then, the amorphous silicon film is crystallized by an action of metal element typified by nickel which promotes crystallization of silicon to obtain a crystalline silicon film. The crystallization is carried out by heat treatment.

This heat treatment is performed within a range of 550°C to 750°C. It is preferable to perform the heat treatment at a temperature above 620°C.

The metal element is contained in the crystalline silicon film in the state in which the film has been crystallized by the above-mentioned heat treatment.

Here, laser light is irradiated to promote the crystallization of the crystalline silicon film obtained and to diffuse (disperse) the nickel element existing within the film further within the film at the same time.

In the state in which the film is crystallized by the first heat treatment, the nickel element exists as certain blocks. Then, the nickel element may be diffused by a certain degree so that it may be readily gettered later by irradiating the laser light described above.

After irradiating the laser light, another heat treatment is performed within an oxidizing atmosphere to which HCl is added to form a thermal oxide film on the surface of the crystalline silicon film.

At this time, the metal element is gettered to the thermal oxide film by the action of chlorine and the concentration of the metal element within the crystalline silicon film

is reduced. Further, the nickel element is gasified and removed to the outside by the action of chlorine.

The heat treatment for gettering the nickel element is preferable to perform at a temperature higher than that of the heat treatment for the crystallization. It is preferable to perform the heat treatment at a temperature over 600°C, or more preferably at 640°C or more. The upper limit thereof may be adequately set as temperature below 750°C.

As a result of the heat treatment for gettering, a thermal oxide film containing the nickel element in high concentration is formed. Then, the crystalline silicon film having the high crystallinity and having low concentration of the metal element may be obtained by removing this thermal oxide film.

The use of the invention disclosed in the present specification allows to provide the technology for reducing the concentration of metal element within the crystalline silicon film which has been obtained by utilizing the metal element which promotes the crystallization of silicon. The use of this technology also allows a more reliable and higher performance thin film semiconductor device to be obtained.

Brief Description of Drawings

FIG. 1 shows steps for obtaining a crystalline silicon film.

FIG. 2 shows steps for obtaining a crystalline silicon film.

FIG. 3 shows steps for fabricating a thin film transistor.

FIG. 4 shows steps for fabricating a thin film transistor.

FIG. 5 shows steps for fabricating a thin film transistor.

FIG. 6 shows steps for fabricating an active layer of the thin film transistor.

FIG. 7 shows states when laser light is irradiated to patterns made of the crystalline silicon film.

Detailed Description of Preferred Embodiments

First Embodiment

An arrangement for obtaining a crystalline silicon film on a glass substrate by utilizing nickel element will be explained in the present embodiment.

At first, the crystalline silicon film having a high crystallinity is obtained by an action of nickel element in the present embodiment.

Then, laser light is irradiated to enhance the crystallinity of the film and to diffuse nickel element existing locally concentrated within the film. That is, the block of nickel is extinguished.

Next, a thermal oxide film containing a halogen element is formed on the crystalline silicon film by thermal oxidation. At this time, the nickel element remaining in the crystalline silicon film thus obtained is gettered to the thermal oxide film by an action of the halogen element. Because the nickel element is distributed by the irradiation of the laser light, the gettering proceeds effectively.

Then, the thermal oxide film containing the nickel element in high concentration

as a result of the gettering is removed. Thereby, the crystalline silicon film having nickel element in low concentration while having the high crystallinity is obtained on the glass substrate.

A fabrication process of the present embodiment will be explained by using FIG. 1. At first, a silicon oxide nitride film 102 is formed as an underlying film in a thickness of 3000 angstrom on the glass substrate 101 of Corning 1737 (distortion point: 667°C).

The silicon oxide nitride film is formed by using plasma CVD using sillane, N_2O gas and oxygen as original gases. Or, it may be formed by using plasma CVD using TEOS gas and N_2O gas.

The silicon oxide nitride film has a function of suppressing the diffusion of impurities from the glass substrate in the later steps (seeing from the level of fabrication of a semiconductor, a glass substrate contains a large amount of impurities).

It is noted that the silicon nitride film is most suitable to maximize the function of suppressing the diffusion of the impurities. However, the silicon nitride film is not practical because it may be peeled off from the glass substrate due to the influence of stress. A silicon oxide film may be also used as the underlying film instead of the silicon oxide nitride film.

It is also important to increase the hardness of the underlying film 102 as much as possible. It is concluded from the fact that the harder the hardness of the underlying film (i.e. the smaller the etching rate thereof), the higher the reliability is in an endurance test of the thin film transistor obtained finally. It is assumed to be caused by the effect of

blocking the impurities from the glass substrate in the fabrication process of the thin film transistor.

It is also effective to include a small amount of halogen element typified by chlorine in the underlying film 102. Thereby, the metal element which promotes crystallization of silicon and which exists within the semiconductor layer may be gettered by the halogen element in the later step.

It is also effective to perform a hydrogen plasma treatment after forming the underlying film. It is also effective to perform a plasma treatment in an atmosphere in which oxygen and hydrogen are mixed. These treatments are effective in removing carbon component which is adsorbed on the surface of the underlying film and in enhancing the interfacial characteristic with a semiconductor film formed later.

Next, an amorphous silicon film 103, which turns out to be a crystalline silicon film later, is formed in a thickness of 500 angstrom by low pressure thermal CVD. The reason why low pressure thermal CVD is used is because the quality of the crystalline silicon film obtained later is better, i.e. the film quality is denser. Besides the low pressure thermal CVD, the plasma CVD may be used.

The amorphous silicon film fabricated here is desirable to have 5×10^{17} cm^{-3} to 2×10^{19} cm^{-3} of concentration of oxygen within the film. It is because oxygen plays an important role in the later step of gettering the metal element (which promotes crystallization of silicon).

However, it must be careful here because the crystallization of the amorphous

silicon film is hampered if the oxygen concentration is higher than the above-mentioned range of concentration.

The concentration of other impurities such as those of nitrogen and carbon is preferred to be as low as possible. In specifically, the concentration must be below 2 x 10^{19} cm^{-3}.

The upper limit of the thickness of the amorphous silicon film is about 2000 angstrom. It is because it is disadvantageous to have a thick film to obtain the effect of laser irradiated later. Thick film is disadvantageous because the laser light irradiated to the silicon film is absorbed almost completely at the surface of the film.

The lower limit of the amorphous silicon film 103 is practically about 200 angstrom, though it depends on how it is formed.

Next, nickel element is introduced to the amorphous silicon film 103 to crystallize it. Here, the nickel element is introduced by applying nickel acetate solution containing 10 ppm (to weight) of nickel on the surface of the amorphous silicon film 103.

Besides the method of using the above-mentioned solution, sputtering, CVD, plasma treatment or adsorption may be used as the method for introducing the nickel element.

The method of using the solution is useful in that it is simple and that the concentration of the metal element may be readily adjusted.

The nickel acetate solution is applied as described above to form a liquid film 104 as shown in FIG. 1A. After obtaining this state, extra solution is blown out by using a

spin coater not shown. Thus, the nickel element is held in contact on the surface of the amorphous silicon film 103.

It is noted that it is preferable to use nickel sulfate solution, instead of using the nickel acetate, if the remained impurities in the later heating process is taken into consideration. It is because the nickel acetate contains carbon and it might be carbonized in the later heating process, thus remaining within the film.

An amount of the nickel element to be introduced may be controlled by adjusting the concentration of nickel element within the solution.

Next, a heat treatment is performed in the temperature range from 550°C to 650°C in the state shown in FIG. 1B to crystallize the amorphous silicon film 103 and to obtain a crystalline silicon film 105. This heat treatment is performed in a reducing atmosphere.

It is preferable to perform the heat treatment below the temperature of the distortion point of the glass substrate. Because the distortion point of the Corning 1737 glass substrate is 667°C, the upper limit of the heating temperature here is preferable to be about 650°C, leaving some margin.

Here, the heat treatment is performed for four hours at 620°C within a nitrogen atmosphere containing 3 % of hydrogen.

The reason why the reducing atmosphere is adopted in the crystallization step by way of the heat treatment is to prevent oxides from being created in the step of the heat treatment and more concretely, to suppress nickel from reacting with oxygen and NiOx from being created on the surface of the film or within the film.

Oxygen couples with nickel and contributes a lot in gettering nickel in the later gettering step. However, it has been found that if oxygen couples with nickel in the above-mentioned stage of the crystallization, it hampers the crystallization. Accordingly, it is important to suppress the oxides from being created to the utmost in the crystallization step carried out by way of heating.

The concentration of oxygen within the atmosphere for performing the heat treatment for the crystallization has to be in an order of ppm, or preferably, less than 1 ppm.

Inert gases such as argon, besides nitrogen, may be used as the gas which occupies the most of the atmosphere for performing the heat treatment for the crystallization.

After the crystallization step by way of the heat treatment, nickel element remains as blocks. This fact has been confirmed from the observation by means of TEM (transmission electron microscope).

Although the cause of the fact that the nickel exists as blocks is not clear yet, it is considered to be related with some crystallization mechanism.

Next, laser light is irradiated as shown in FIG. 1C. Here, KrF excimer laser (wavelength: 248 nm) is used. Here, a method of irradiating the laser light by scanning its linear beam is adopted.

The nickel element which has been locally concentrated as a result of the crystallization carried out by way of the aforementioned heat treatment is distributed by a certain degree within the film 105 by irradiating the laser light. That is, the nickel

element may be distributed by disappearing the blocks of the nickel element.

Another heat treatment is performed in the step shown in FIG. 1D to form a thermal oxide film for gettering the nickel element. Here, this heat treatment is performed within an atmosphere containing halogen element. Specifically, the heat treatment is carried out in an oxygen atmosphere containing 5 % of HCl (FIG. 1D).

This step is carried out to remove the nickel element (or another element which promotes crystallization of silicon) which has been introduced intentionally for the crystallization in the initial stage from the crystalline silicon film 105. This heat treatment is performed at a temperature higher than that of the heat treatment performed for the crystallization described above. It is an important condition for effectively performing the gettering of nickel element.

This heat treatment is performed in the temperature range from 600°C to 750°C upon meeting the above-mentioned condition. The effect of gettering the nickel element in this step may be obtained remarkably when the temperature is higher than 600°C.

In this step, the nickel element which has been distributed by the above-mentioned irradiation of laser is effectively gettered to the oxide film.

Further, the upper limit of the heating temperature is limited by the distortion point of the glass substrate to be used. It must be careful not to perform the heat treatment in a temperature above the distortion point of the glass substrate to be used because it is deformed.

It is preferable to mix HCl with a ratio of 0.5 % to 10 % (volume %) of oxygen.

It must be careful not to mix it above this concentration because, otherwise, the surface of the film is roughened with the same degree of irregularity with the thickness of the film.

By performing the heat treatment under such conditions, the thermal oxide film 106 containing chlorine as shown in FIG. 1D is formed. Here, the heat treatment is performed for 12 hours and the thickness of the thermal oxide film 106 is 100 angstrom.

Because the thermal oxide film 106 is formed, the thickness of the crystalline silicon film 103 becomes about 450 angstrom.

When the heating temperature is 600°C to 750°C in this heat treatment, the treatment time (heating time) is set at 10 hours to 48 hours, typically at 24 hours.

This treatment time may be set adequately depending on the thickness of the oxide film to be obtained as a matter of course.

In this step, nickel element is gettered out of the silicon film by the action of the halogen element. Here, the nickel element is gettered to the thermal oxide film 106 formed by the action of chlorine.

In the gettering, oxygen existing within the crystalline silicon film plays an important role. That is, the gettering of the nickel element proceeds effectively by chlorine acting on nickel oxide formed when oxygen couples with nickel.

If the concentration of oxygen is too much, it becomes the factor of hampering the crystallization of the amorphous silicon film 103 in the crystallization step shown in FIG. 1B as described above. However, the existence thereof plays an important role in the

process of gettering nickel as described above. Accordingly, it is important to control the concentration of oxygen existing within the amorphous silicon film as a starting film.

Here, Cl has been selected as the halogen element and the case of using HCl has been shown as a method for introducing it. Besides HCl, one type or a plurality of types of mixed gas selected from HF, HBr, Cl_2, F_2, Br_2 may be used. Besides them, halogen hydroxide may be used in general.

It is preferable to set the content (volume content) of those gases within the atmosphere to 0.25 to 5 % if it is HF, 1 to 15 % if it is HBr, 0.25 to 5 % if it is Cl_2, 0.125 to 2.5 % if it is F_2 and 0.5 to 10 % if it is Br_2.

If the concentration is below the above-mentioned range, no significant effect is obtained. Further, if the concentration exceeds the upper limit of the above-mentioned range, the surface of the crystalline silicon film is roughened.

Through this step, the concentration of nickel element may be reduced to less than 1/10 of the maximum from the initial stage. It means that the nickel element may be reduced to 1/10 as compared to the case when no gettering by the halogen element is conducted. This effect may be obtained in the same manner even when another metal element is used.

Because the nickel element is gettered to the oxide film formed in the above-mentioned step, naturally the nickel concentration within the oxide film becomes high as compared to other regions.

Further, it has been observed that the concentration of nickel element is apt to be

high near the interface of the crystalline silicon film 105 with the oxide film 106. It is considered to happen because the region where the gettering mainly takes place is on the side of the oxide film near the interface between the silicon film and the oxide film. The gettering proceeding near the interface is considered to be caused by the existence of stress and defects.

Then, the thermal oxide film 106 containing nickel in high concentration is removed. The thermal oxide film 106 may be removed by means of wet etching or dry etching using buffered hydrofluoric acid (or other hydrofluorite etchant).

Thus, a crystalline silicon film 107 in which the concentration of nickel has been reduced is obtained as shown in FIG. 1E.

Because nickel element is contained near the surface of the obtained crystalline silicon film 107 in relatively high concentration, it is effective to advance the above-mentioned etching to over-etch, more or less, the surface of the crystalline silicon film 107.

It is also effective to irradiate laser light again after removing the thermal oxide film 106 to promote the crystallinity of the crystalline silicon film 107 thus obtained further. That is, it is effective to irradiate laser light again after gettering the nickel element.

Although the case when the KrF excimer laser (wavelength: 248 nm) is used as the laser to be used has been shown in the present specification, it is possible to use a XeCl excimer laser (wavelength: 308 nm) and other types of excimer lasers.

It is also possible to arrange so as to irradiate ultraviolet rays or infrared rays for example instead of laser light.

Second Embodiment

The present embodiment relates to a case when Cu is used as the metal element which promotes the crystallization of silicon in the arrangement shown in the first embodiment. In this case, cupric acetate [$Cu(CH_3\ COO)_2$] or cupricchloride ($CuCl_2$ $2H_2O$) may be used as the solution for introducing Cu.

Third Embodiment

The present embodiment relates to a case of growing crystal in the form different from that in the first embodiment. That is, the present embodiment relates to a method of growing the crystal in a direction parallel to the substrate, i.e. a method called lateral growth, by utilizing the metal element which promotes crystallization of silicon.

FIG. 2 shows the fabrication process according to the present embodiment. At first, a silicon oxide nitride film is formed as an underlying film 202 in a thickness of 3000 angstrom on the Corning 1737 glass substrate (or a quartz substrate) 201.

Next, an amorphous silicon film 203 which is the starting film for a crystalline silicon film is formed in a thickness of 600 angstrom by low pressure thermal CVD. The thickness of the amorphous silicon film is preferable to be less than 2000 angstrom as described before.

It is noted that plasma CVD may be used instead of the low pressure thermal CVD.

Next, a silicon oxide film not shown is formed in a thickness of 1500 angstrom and is patterned to form a mask 204. An opening is created on the mask in a region 205. The amorphous silicon film 203 is exposed at the region where the opening 205 is created.

The opening 205 has a thin and long rectangular shape in the longitudinal direction from the depth to the front side of the figure. Preferably, the width of the opening 203 is 20 μm or more. The length thereof in the longitudinal direction may be determined arbitrarily.

Then, the nickel acetate aqueous solution containing 10 ppm of nickel element in terms of weight is applied in the same manner with the first embodiment and the extra solution is removed by performing spin drying by using a spinner not shown.

Thus, the solution is held in contact on the exposed surface of the amorphous silicon film 203 as indicated by a dotted line 206 in FIG. 2A.

Next, a heat treatment is performed at 640°C for four hours in a nitrogen atmosphere containing 3 % of hydrogen and in which oxygen is minimized. Then, crystal grows in the direction parallel to the substrate as indicated by the reference numeral 207 in FIG. 2B. This crystal growth advances from the region of the opening 205 to which nickel element has been introduced to the surrounding part. This crystal growth in the direction parallel to the substrate will be referred to as lateral growth.

It is possible to advance this lateral growth across more than 100 μm under the conditions shown in the present embodiment. Then, a silicon film 208 having a region in which the crystal has thus grown laterally is obtained. It is noted that crystal growth in the vertical direction called vertical growth advances from the surface of the silicon film to the underlying interface in the region where the opening 205 is formed.

Then, the mask 204 made of the silicon oxide film for selectively introducing nickel element is removed. Thus, the state shown in FIG. 2C is obtained. In this state, the vertical growth region, the lateral growth region and a region in which no crystal has grown (having amorphous state) exist within the silicon film 208.

In this state, the nickel element is unevenly distributed in the film. In particular, the nickel element exists in relatively high concentration at the region where the opening 205 has been formed and at the edge portion 207 of the crystal growth.

After obtaining the state shown in FIG. 2C, laser light is irradiated. The KrF excimer laser is irradiated here similarly to the first embodiment.

The nickel element which has been unevenly distributed is diffused in this step to obtain a condition in which it can be gettered readily in the later gettering step.

After irradiating the laser light, a heat treatment is performed at 650°C for 12 hours within an oxygen atmosphere containing 3 % of HCl. In this step, an oxide film 209 containing nickel element in high concentration is formed. In the same time, the concentration of nickel element within the silicon film 208 may be reduced relatively (FIG. 2D).

Here, the thermal oxide film 209 is formed in a thickness of 100 angstrom. The thermal oxide film contains the nickel element thus gettered by the action of chlorine in high concentration. Further, because the thermal oxide film 209 is formed, the thickness of the crystalline silicon film 208 is reduced to about 500 angstrom.

Next, the thermal oxide film 209 containing nickel element in high concentration is removed.

In the crystalline silicon film of this state, the nickel element has a distribution of concentration such that it exists in high concentration toward the surface of the crystalline silicon film. This state is caused by the fact that the nickel element has been gettered to the thermal oxide film 209 when the thermal oxide film was formed.

Accordingly, it is useful to etch the surface of the crystalline silicon film to remove the region in which the nickel element exists in high concentration after removing the thermal oxide film 209. That is, the crystalline silicon film in which the nickel element concentration is reduced further may be obtained by etching the surface of the crystalline silicon film in which the nickel element exists in high concentration. However, it is necessary to consider the thickness of the silicon film finally obtained at this time.

Next, patterning is performed to form a pattern 210 formed of the laterally grown region.

The concentration of nickel element which remains within the pattern 210 made of the lateral growth region thus obtained may be reduced further as compared to the case shown in the first embodiment.

This is caused by the fact that the concentration of the metal element contained within the lateral growth region is low originally. Specifically, the concentration of nickel element within the pattern 209 made of the lateral growth region may be readily reduced to the order of 10^{17} cm^{-3} or less.

When a thin film transistor is formed by utilizing the lateral growth region, a semiconductor device having a higher mobility may be obtained as compared to the case when the vertical growth region as shown in the first embodiment (crystal grows vertically on the whole surface in the case of the first embodiment) is utilized.

It is noted that it is useful to perform the etching process further after forming the pattern shown in FIG. 2E to remove the nickel element existing on the surface of the pattern.

Then, a thermal oxide film 211 is formed after forming the pattern 210. This thermal oxide film is formed into a thickness of 200 angstrom by performing a heat treatment for 12 hours in an oxygen atmosphere at 650°C.

This thermal oxide film becomes a part of a gate insulating film later when a thin film transistor is constructed.

If the thin film transistor is to be fabricated thereafter, a silicon oxide film is formed further by means of plasma CVD or the like so as to cover the thermal oxide film 211 to form a gate insulating film.

Fourth Embodiment

The present embodiment relates to a case of fabricating a thin film transistor disposed in a pixel region of an active matrix type liquid crystal display or an active matrix type EL display by utilizing the invention disclosed in the present specification.

FIG. 3 shows the fabrication process according to the present embodiment. At first, the crystalline silicon film is formed on the glass substrate through the process shown in the first or the third embodiment. When the crystalline silicon film is obtained by the arrangement shown in the first embodiment, it is patterned to obtain the state shown in FIG. 3A.

In the state shown in FIG. 3A, the reference numeral 301 denotes a glass substrate, 302 an underlying film, and 303 an active layer formed of the crystalline silicon film. After obtaining the state shown in FIG. 3A, a plasma treatment is performed within a reduced pressure atmosphere in which oxygen and hydrogen are mixed. The plasma is generated by high-frequency discharge.

Organic substances existing on the surface of the exposed active layer 303 may be removed by the above-mentioned plasma treatment. To be exact, the organic substances adsorbing on the surface of the active layer are oxidized by oxygen plasma and the oxidized organic substances are reduced and vaporized further by hydrogen plasma. Thus the organic substances existing on the surface of the exposed active layer 303 are removed.

The removal of the organic substances is very effective in suppressing fixed charge from existing on the surface of the active layer 303. Because the fixed charge caused by

the existence of organic substances hampers the operation of the device and renders the characteristics thereof instable, it is very useful to reduce it.

After removing the organic substances, thermal oxidation is performed within an oxygen atmosphere at 640°C to form a thermal oxide film 300 of 100 angstrom thick. This thermal oxide film has a high interfacial characteristic with a semiconductor layer and composes a part of a gate insulating film later. Thus, the state shown in FIG. 3A is obtained.

After obtaining the state shown in FIG. 3A, a silicon oxide nitride film 304 which composes the gate insulating film is formed in a thickness of 1000 angstrom. The film may be formed by using plasma CVD using mixed gas of oxygen, sillane and N_2O or plasma CVD using mixed gas of TEOS and N_2O.

The silicon oxide nitride film 304 functions as the gate insulating film together with the thermal oxide film 300.

It is also effective to contain halogen element within the silicon oxide nitride film. That is, by fixing the nickel element by the action of the halogen element, it is possible to prevent the function of the gate insulating film as an insulating film from being reduced by the influence of the nickel element (or another metal element which promotes crystallization of silicon) existing within the active layer.

It is significant to use the silicon oxide nitride film in that the metal element hardly infiltrates to the gate insulating film because of its dense film quality. If the metal element infiltrates into the gate insulating film, its function as an insulating film is

reduced, thus causing instability and dispersion of characteristics of the thin film transistor.

It is noted that a silicon oxide film which is normally used may be also used for the gate insulating film.

After forming the silicon oxide nitride film 304 which functions as the gate insulating film, an aluminum film not shown which functions as a gate electrode later is formed by sputtering. Scandium is included 0.2 weight % of aluminum within the aluminum film.

Scandium is included in the aluminum film to suppress hillock and whisker from being generated in the later process. The hillock and whisker mean that abnormal growth of aluminum occurs by heating, thus forming needle or prickle-like projections.

After forming the aluminum film, a dense anodic oxide film not shown is formed. The anodic oxide film is formed by using ethylene glycol solution containing 3 % of tartaric acid as electrolyte. That is, the anodic oxide film having the dense film quality is formed on the surface of the aluminum film by setting the aluminum film as the anode and platinum as the cathode and by anodizing within this electrolyte.

The thickness of the anodic oxide film not shown having the dense film quality is around 100 angstrom. This anodic oxide film plays a role of enhancing the adhesiveness with a resist mask to be formed later.

It is noted that the thickness of the anodic oxide film may be controlled by adjusting voltage applied during the anodization.

Next, the resist mask 306 is formed and the aluminum film is patterned so as to have a pattern 305. The state shown in FIG. 3B is thus obtained.

Here, another anodization is performed. In this case, 3 % of oxalate aqueous solution is used as electrolyte. A porous anodic oxide film 308 is formed by anodizing within this electrolyte by setting the aluminum pattern 305 as the anode.

In this step, the anodic oxide film 308 is formed selectively on the sides of the aluminum pattern because the resist mask 306 having the high adhesiveness exists thereabove.

The anodic oxide film may be grown up to severalμm thick. The thickness is 6000 angstrom here. It is noted that the range of the growth may be controlled by adjusting an anodizing time.

Next, the resist mask 306 is removed. Then, a dense anodic oxide film is formed again. That is, the anodization is performed again by using the ethylene glycol solution containing 3 % of tartaric acid as electrolyte. Then, an anodic oxide film 309 having a dense film quality is formed because the electrolyte infiltrates into the porous anodic oxide film 308.

This dense anodic oxide film 309 is 1000 angstrom thick. The thickness is controlled by adjusting applied voltage.

Here, the exposed silicon oxide nitride film 304 and the thermal oxide film 300 are etched by utilizing dry etching. Then, the porous anodic oxide film 308 is removed by using mixed acid in which acetic acid, nitric acid and phosphoric acid are mixed.

Thus, the state shown in FIG. 3D is obtained.

After obtaining the state shown in FIG. 3D, impurity ions are implanted. Here, P (phosphorus) ions are implanted by plasma doping in order to fabricate an N-channel type thin film transistor.

In this step, heavily doped regions 311 and 315 and lightly doped regions 312 and 314 are formed because part of the remaining silicon oxide film 310 functions as a semi-permeable mask, thus blocking part of the implanted ions.

Then, laser light or intense light is irradiated to activate the regions into which the impurity ions have been implanted. Thus, a source region 311, a channel forming region 313, a drain region 315 and low concentration impurity regions 312 and 314 are formed in a manner of self-alignment.

One designated by the reference numeral 314 here is the region called the LDD (lightly doped region) (FIG. 3D).

It is noted that when the dense anodic oxide film 309 is formed as thick as 2000 angstrom or more, offset gate regions may be formed on the outside of the channel forming region 313 by its thickness.

Although the offset gate regions are formed also in the present embodiment, it is not shown in the figures because its size is small, its contribution due to the existence thereof is small and because the figures might otherwise become complicated.

Next, a silicon oxide film or a silicon nitride film or their laminated film is formed as an interlayer insulating film 316. The interlayer insulating film may be constructed

by forming a layer made of a resin material on the silicon oxide film or the silicon nitride film.

Then, contact holes are created to form a source electrode 317 and a drain electrode 318. Thus, the thin film transistor shown in FIG. 3E is completed.

Fifth Embodiment

The present embodiment relates to a method for forming the gate insulating film 304 in the arrangement shown in the fourth embodiment. Thermal oxidation may be used as a method for forming the gate insulating film when a quartz substrate or a glass substrate having a high heat resistance is used as the substrate.

The thermal oxidation allows the film quality to be densified and is useful in obtaining a thin film transistor having stable characteristics.

That is, because an oxide film formed by the thermal oxidation is dense as an insulating film and movable electric charge existing therein can be reduced, it is one of the most suitable films as a gate insulating film.

As the method for forming the thermal oxide film, a heat treatment performed in an oxidizing atmosphere at 950°C may be cited.

At this time, it is effective to mix HCl or the like within the oxidizing atmosphere. Thereby, the metal element existing within the active layer may be fixed in the same time with the formation of the thermal oxide film.

It is also effective to form a thermal oxide film containing nitrogen component by

mixing N_2O gas within the oxidizing atmosphere. Here, it is possible to obtain a silicon oxide nitride film by the thermal oxidation by optimizing the mixed ratio of the N_2O gas.

It is noted that the thermal oxide film 300 needs not be always formed in the present embodiment.

Sixth Embodiment

The present embodiment relates to a case of fabricating a thin film transistor through a process different from that shown in FIG. 3.

FIG. 4 shows the fabrication process according to the present embodiment. At first, the crystalline silicon film is formed on the glass substrate through the process shown in the first or third embodiment. It is then patterned, thus obtaining the state shown in FIG. 4A.

After obtaining the state shown in FIG. 4A, a plasma treatment is performed within a reduced pressure atmosphere in which oxygen and hydrogen are mixed.

In the state shown in FIG. 4A, the reference numeral 401 denotes a glass substrate, 402 an underlying film, 403 an active layer made of the crystalline silicon film and 400 a thermal oxide film formed again after removing the thermal oxide film for gettering.

After obtaining the state shown in FIG. 4A, a silicon oxide nitride film 404 which composes a gate insulating film is formed in a thickness of 1000 angstrom. The film may be formed by using plasma CVD using mixed gas of oxygen, sillane and N_2O or plasma CVD using mixed gas of TEOS and N_2O.

The silicon oxide nitride film 404 composes the gate insulating film together with the thermal oxide film 400. It is noted that a silicon oxide film may be used besides the silicon oxide nitride film.

After forming the silicon oxide nitride film 404 which functions as the gate insulating film, an aluminum film (not shown) which functions as a gate electrode later is formed by sputtering. Scandium is included within the aluminum film at 0.2 weight %.

After forming the aluminum film, a dense anodic oxide film not shown is formed. The anodic oxide film is formed by using ethylene glycol solution containing 3 % of tartaric acid as electrolyte. That is, the anodic oxide film having the dense film quality is formed on the surface of the aluminum film by setting the aluminum film as the anode and platinum as the cathode and by anodizing within this electrolyte.

The thickness of the anodic oxide film not shown having the dense film quality is about 100 angstrom. This anodic oxide film plays a role of enhancing the adhesiveness with a resist mask to be formed later.

It is noted that the thickness of the anodic oxide film may be controlled by adjusting voltage applied during the anodization.

Next, the resist mask 405 is formed and the aluminum film is patterned so as to have a pattern 406.

Here, another anodization is performed. In this case, 3 % of oxalate aqueous solution is used as electrolyte. A porous anodic oxide film 407 is formed by anodizing

within this electrolyte by setting the aluminum pattern 406 as the anode.

In this step, the anodic oxide film 407 is formed selectively on the sides of the aluminum pattern because the resist mask 405 having the high adhesiveness exists thereabove.

The anodic oxide film may be grown up to several μm thick. The thickness is 6000 angstrom here. It is noted that the range of the growth may be controlled by adjusting an anodizing time.

Then, the resist mask 405 is removed and another dense anodic oxide film is formed. That is, the anodization is performed again by using the ethylene glycol solution containing 3 % of tartaric acid as electrolyte. Then, an anodic oxide film 408 having a dense film quality is formed because the electrolyte infiltrates into the porous anodic oxide film 407 (FIG. 2C).

Here, the initial implantation of impurity ions is performed. This step may be performed after removing the resist mask 405.

A source region 409 and a drain region 411 are formed by implanting the impurity ions. No impurity ion is implanted to a region 410.

Then, the porous anodic oxide film 407 is removed by using mixed acid in which acetic acid, nitric acid and phosphoric acid are mixed. Thus, the state shown in FIG. 4D is obtained.

After obtaining the state shown in FIG. 4D, impurity ions are implanted again. The impurity ions are implanted under the doping condition lighter than that of the first

implantation.

In this step, lightly doped regions 412 and 413 are formed and a region 414 turns out to be a channel forming region (FIG. 4D).

Then, laser light or intense light is irradiated to activate the regions into which the impurity ions have been implanted. Thus, the source region 409, the channel forming region 414, the drain region 411 and low concentration impurity regions 412 and 413 are formed in a manner of self-alignment.

Here, one designated by the reference numeral 413 is the region called the LDD (lightly doped region) (FIG. 4D).

Next, a silicon oxide film or a silicon nitride film or their laminated film is formed as an interlayer insulating film 414. The interlayer insulating film may be constructed by forming a layer made from a resin material on the silicon oxide film or the silicon nitride film.

After that, contact holes are created to form a source electrode 416 and a drain electrode 417. Thus, the thin film transistor shown in FIG. 4E is completed.

Seventh Embodiment

The present embodiment relates to a case when an N-channel type thin film transistor and a P-channel type thin film transistor are formed in a complementary manner.

The arrangement shown in the present embodiment may be utilized for various thin

film integrated circuits integrated on an insulated surface as well as for peripheral driving circuits of an active matrix type liquid crystal display for example.

At first, a silicon oxide film or a silicon oxide nitride film is formed as an underlying film 502 on a glass substrate 501 as shown in FIG. 5A. It is preferable to use the silicon oxide nitride film.

Next, an amorphous silicon film not shown is formed by plasma CVD or low pressure thermal CVD. Then, the amorphous silicon film is transformed into a crystalline silicon film by the same method as shown in the first embodiment.

Next, a plasma treatment is performed within an atmosphere in which oxygen and hydrogen are mixed. Then, the obtained crystalline silicon film is patterned to obtain active layers 503 and 504. Thus, the state shown in FIG. 5A is obtained.

It is noted that a heat treatment of ten hours at 650°C is performed within a nitrogen atmosphere containing 3 % of HCl in the state shown in FIG. 5A in order to suppress the influence of carriers moving the side of the active layer.

Because an OFF current characteristic is degraded if a trap level exists on the side of the active layer due to the existence of the metal element, it is useful, by performing the process shown here, to reduce the density of the level on the side of the active layer.

Further, the thermal oxide film 500 and the silicon oxide nitride film 505 which compose a gate insulating film are formed. If quartz is used as the substrate here, it is desirable to compose the gate insulating film only by the thermal oxide film formed by using the above-mentioned thermal oxidation.

Next, an aluminum film not shown which composes a gate electrode later is formed in a thickness of 4000 angstrom. Besides the aluminum film, a metal which can be anodized (e.g. tantalum) may be used.

After forming the aluminum film, a very thin and dense anodic oxide film is formed on the surface thereof by the method described before.

Next, a resist mask not shown is provided on the aluminum film to pattern the aluminum film. Then, anodization is performed by setting the obtained aluminum pattern as the anode to form porous anodic oxide films 508 and 509. The thickness of the porous anodic oxide films is 5000 angstrom for example.

Then, another anodization is performed under the condition of forming dense anodic oxide films to form dense anodic films 510 and 511. The thickness of the dense anodic oxide films 510 and 511 is 800 angstrom. Thus, the state shown in FIG. 5B is obtained.

Then, the exposed silicon oxide film 505 and the thermal oxide film 500 are removed by dry etching, thus obtaining the state shown in FIG. 5C.

After obtaining the state shown in FIG. 5C, the porous anodic oxide films 508 and 509 are removed by using mixed acid in which acetic acid, nitric acid and phosphoric acid are mixed. Thus, the state shown in FIG. 5D is obtained.

Here, resist masks are disposed alternately to implant P ions to the thin film transistor on the left side and B ions to the thin film transistor on the right side.

By implanting those impurity ions, a source region 514 and a drain region 517

having N-type in high concentration are formed in a manner of self-alignment.

Further, a region 515 to which P ions are doped in low concentration, thus having weak N-type, as well as a channel forming region 516 are formed in the same time.

The reason why the region 515 having the weak N-type is formed is because the remaining gate insulating film 512 exists. That is, part of P ions transmitting through the gate insulating film 512 is blocked by the gate insulating film 512.

By the same principle, a source region 521 and a drain region 518 having strong P-type are formed in a manner of self-alignment and a low concentrate impurity region 520 is formed in the same time. Further, a channel forming region 519 is formed in the same time.

In the case that when the thickness of the dense anodic oxide films 510 and 511 is as thick as 2000 angstrom, an offset gate region may be formed in contact with the channel forming region by that thickness.

Its existence may be ignored in the case of the present embodiment because the dense anodic oxide films 510 and 511 are so thin as less than 1000 angstrom.

Then, laser light or intense light is irradiated to anneal the region into which the impurity ions have been implanted.

Then, a silicon nitride film 522 and a silicon oxide film 523 are formed as interlayer insulating films as shown in FIG. 5E. The thickness is 1000 angstrom, respectively. It is noted that the silicon oxide film 523 need not be formed.

Here, the thin film transistor is covered by the silicon nitride film. The reliability

of the thin film transistor may be enhanced by arranging as described above because the silicon nitride film is dense and has a favorable interfacial characteristic.

Further, an interlayer insulating film 524 made of a resin material is formed by means of spin coating. Here, the thickness of the interlayer insulating film 524 is 1 μm (FIG. 5E).

Then, contact holes are created to form a source electrode 525 and a drain electrode 526 of the N-channel type thin film transistor on the left side. In the same time, a source electrode 527 and the drain electrode 526 of the thin film transistor on the right side are formed. Here, the electrode 526 is disposed in common.

Thus, the thin film transistor circuit having a CMOS structure constructed in a complementary manner may be formed.

According to the arrangement shown in the present embodiment, the thin film transistor is covered by the nitride film and further the resin material. This arrangement allows to enhance the durability of the thin film transistor to which movable ions nor moisture hardly infiltrate.

Further, it allows to prevent capacitance from being generated between the thin film transistor and wires when a multi-layered wire is formed.

Eighth Embodiment

The present embodiment relates to a case when nickel element is introduced directly to the surface of the underlying film in the process shown in the first

embodiment. In this case, the nickel element is held in contact with the lower surface of the amorphous silicon film.

In this case, nickel element is introduced after forming the underlying film such that the nickel element (metal element) is held in contact with the surface of the underlying film. Besides the method of using the solution, sputtering, CVD or adsorption may be used as the method for introducing nickel element.

Ninth Embodiment

The present embodiment is characterized in that the crystallinity of an island pattern formed of a crystalline silicon film in the state shown in FIG. 2E, the state shown in FIG. 3A or the state shown in FIG. 4A is improved by irradiating laser light.

A predetermined annealing effect can be obtained with relatively low irradiation energy density by irradiating the laser light in the state shown in FIGs. 2E, 3A and 4A.

It is considered to have been effected because the laser energy is irradiated to a spot of small area, thus enhancing the efficiency of energy utilized in the annealing.

Tenth Embodiment

The present embodiment relates to a case in which patterning of an active layer of a thin film transistor is devised in order to enhance the effect of annealing by the irradiation of laser light.

FIG. 6 shows a process for fabricating the thin film transistor according to the

present embodiment. At first, a silicon oxide film or silicon oxide nitride film is formed as an underlying layer on a Corning 1737 glass substrate 601.

Next, an amorphous silicon film not shown is formed in a thickness of 500 angstrom by using low pressure thermal CVD. It is noted that this amorphous silicon film turns out to be a crystalline silicon film 603 through the crystallization process later.

Next, the amorphous silicon film not shown is crystallized by the method shown in the first embodiment (see FIG. 1) or third embodiment (see FIG. 2) to obtain the crystalline silicon film. Thus, the state shown in FIG. 6A is obtained.

After obtaining the state shown in FIG. 6A, the crystalline silicon film 603 is formed on the glass substrate in accordance to the process shown in the first embodiment whose fabrication process is shown in FIG. 1 or the third embodiment whose fabrication process is shown in FIG. 2. That is, the amorphous silicon film is crystallized by the heat treatment using nickel element to obtain the crystalline silicon film 604. The heat treatment is performed at 620°C for four hours.

After obtaining the crystalline silicon film, a pattern for constructing an active layer of a thin film transistor is formed. At this time, the pattern is formed so as to have a sectional profile 604 shown in FIG. 6B.

The pattern 604 as shown in FIG. 6B is formed in order to suppress the shape of the pattern from being deformed in the later treatment step of irradiating laser light.

In general, when laser light is irradiated to a pattern 702 made of a normal island-shape silicon film formed on a base 701 as shown in FIG. 7A, a convex portion 704 is

formed at the edge of a pattern 703 after the irradiation of the laser light as shown in FIG. 7B.

It is considered to happen because energy of the irradiated laser light is concentrated at the edge of the pattern where heat cannot be released.

This phenomenon may become a factor of defective wires composing a thin film transistor or of defective operation thereof later.

Thus, the pattern 604 of the active layer is formed so as to have the profile as shown in FIG. 6B in the arrangement of the present embodiment.

Such arrangement allows to suppress the pattern of the silicon film from being deformed like the one shown in FIG. 7B when laser light is irradiated.

It is preferable to set an angle of the part designated by the reference numeral 605 from 20° to 50°. It is not preferable to set the angle of 605 below 20° because an area occupied by the active layer increases and it becomes difficult to form it. Further, it is not also preferable to set the angle of 600 above 50° because the effect for suppressing the shape as shown in FIG. 7B from being formed is reduced.

The pattern 604 may be realized by utilizing isotropic dry etching in patterning it and by controlling the conditions of this dry etching.

After obtaining the pattern (which turns out to be the active layer later) having the shape 603 in FIG. 6B, laser light is irradiated as shown in FIG. 6C. This step allows to diffuse the nickel element which is locally blocked within the pattern 604 and to promote the crystallization of the pattern.

After finishing to irradiate laser light, a heat treatment is performed within an oxygen atmosphere containing 3 % of HCl to form a thermal oxide film 606. Here, the thermal oxide film is formed in 100 angstrom thick by performing the heat treatment for 12 hours in the oxygen atmosphere containing 3 % of HCl at 650°C (FIG. 6D).

The nickel element contained in the pattern 604 is gettered to the thermal oxide film by the action of chlorine. At this time, because the block of the nickel element has been destroyed through the irradiation of laser light in the previous step, the gettering of the nickel element is effectively performed.

Further, the gettering is performed also from the side surfaces of the pattern 604 when the arrangement shown in the present embodiment is adopted. This is useful in enhancing the OFF current characteristics and the reliability of the thin film transistor finally completed. It is because the existence of nickel element which promotes crystallization of silicon and which exists in the side of the active layer relates a wide influence over the increase of OFF current and the instability of the characteristics.

After forming the thermal oxide film 606 for gettering as shown in FIG. 6D, the thermal oxide film 606 is removed. Thus, the state shown in FIG. 6E is obtained. It is concerned that the silicon oxide film 602 might be etched in the step of removing the thermal oxide film 606 when the silicon oxide film is adopted as the underlying layer 602. However, it does not matter so much when the thickness of the thermal oxide film 606 is as thin as 100 angstrom as shown in the present embodiment.

After obtaining the state shown in FIG. 6E, a new thermal oxide film 607 is

formed by a heat treatment in an atmosphere of 100 % oxygen.

Here, the thermal oxide film 607 is formed in a thickness of 100 angstrom by the heat treatment in the oxygen atmosphere at 650°C.

The thermal oxide film 607 is effective in suppressing the surface of the pattern 603 from being roughened when the laser light is irradiated later. The thermal oxide film also forms a part of a gate insulating film later. Because the thermal oxide film has a very favorable interfacial characteristic with the crystalline silicon film, it is useful to utilize it as part of the gate insulating film.

The laser light may be irradiated again after forming the thermal oxide film 607. Thus, the crystalline silicon film 604 in which the concentration of nickel element has been reduced and which has a high crystallinity may be obtained.

Thereafter, the thin film transistor is fabricated by performing through the process shown in FIG. 3 or 4.

Eleventh Embodiment

The present embodiment relates to a case devised in applying a heat treatment at a temperature more than a distortion point of a glass substrate. It is preferable to perform the process for gettering the metal element which promotes crystallization of silicon in the present invention disclosed in the present specification at a high temperature as much as possible.

When the Corning 1737 glass substrate (distortion point: 667°C) is used for

instance, the higher gettering effect can be obtained when the temperature in gettering nickel element by forming the thermal oxide film is 700°C rather than when it is 650°C.

However, if the heating temperature for forming the thermal oxide film is set at 700°C using the Corning 1737 glass substrate, the glass substrate deforms as a result.

The present embodiment provides means for solving this problem. That is, according to the arrangement shown in the present embodiment, the glass substrate is placed on a lapping plate which is formed of quartz whose flatness is guaranteed and the heat treatment is performed in this state.

Thereby, the flatness of the softened glass substrate is maintained by the flatness of the lapping plate. It is noted that it is also important to perform cooling in the state in which the glass substrate is placed on the lapping plate.

The adoption of such arrangement allows the heat treatment to be performed even if it is at the temperature above the distortion point of the glass substrate.

WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film on an insulating surface;

forming a semiconductor island having a tapered shape by patterning said semiconductor film, said tapered shape having an angle within a range of 20° to 50° between a side thereof and an underlying surface; and

irradiating a laser light to said semiconductor island.

2. A method according to claim 1, wherein said semiconductor film is crystalline semiconductor film.

3. A method according to claim 1, wherein said patterning is performed by an isotropic dry etching method.

4. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film on an insulating surface;

crystallizing said semiconductor film by heating;

forming a semiconductor island having a tapered shape by patterning the crystallized semiconductor film, said tapered shape having an angle within a range of 20° to 50° between a side thereof and an underlying surface; and

irradiating a laser light to said semiconductor island.

5. A method according to claim 4, wherein said heating is performed at a temperature of 550 to 750°C.

6. A method according to claim 4, wherein said patterning is performed by an isotropic dry etching method.

7. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film on an insulating surface;

providing a crystallization promoting material onto said semiconductor film;

crystallizing said semiconductor film by heating;

forming a semiconductor island having a tapered shape by patterning the crystallized semiconductor film, said tapered shape having an angle within a range of 20°to 50°between a side thereof and an underlying surface; and

irradiating a laser light to said semiconductor island.

8. A method according to claim 7, wherein said heating is performed at a temperature of 550 to 750 °C.

9. A method according to claim 7, wherein said patterning is performed by an isotropic dry etching method.

10. A method according to claim 7, wherein said crystallization promoting material is selected form the group consisting of Fe, Co, Ni, Ru, Rh, Pd, OS, Ir, Pt, Cu and Au.

11. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film on an insulating surface;

crystallizing said semiconductor film by a first heating;

forming a semiconductor island having a tapered shape by patterning the crystallized semiconductor film, said tapered shape having an angle within a range of 20°to 50°between a side thereof and an underlying surface;

irradiating a laser light to said semiconductor island; and

forming a silicon oxide film on a surface of said semiconductor island by a second heating.

12. A method according to claim 11, wherein said first heating is performed at a temperature of 550 to 750°C.

13. A method according to claim 11, wherein said patterning is performed by an isotropic dry etching method.

14. A method according to claim 11, wherein said second heating is performed at a temperature higher than said first heating.

15. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film on an insulating surface;

providing a crystallization promoting material onto said semiconductor film;

crystallizing said semiconductor film by a first heating;

forming a semiconductor island having a tapered shape by patterning the crystallized semiconductor film, said tapered shape having an angle within a range of 20°to 50° between a side thereof and an underlying surface;

irradiating a laser light to said semiconductor island; and

forming a silicon oxide film on a surface of said semiconductor island by a second heating.

16. A method according to claim 15, wherein said first heating is performed at a temperature of 550 to 750°C.

17. A method according to claim 15, wherein said patterning is performed by an isotropic dry etching method.

18. A method according to claim 15, wherein said second heating is performed at a temperature higher than said first heating.

19. A method according to claim 15, wherein said crystallization promoting material is selected form the group consisting of Fe, Co, Ni, Ru, Rh, Pd, OS, Ir, Pt, Cu and Au.

20. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film on an insulating surface;

providing a crystallization promoting material onto said semiconductor film;

crystallizing said semiconductor film by a first heating;

forming a semiconductor island having a tapered shape by patterning the crystallized semiconductor film, said tapered shape having an angle within a range of 20°to 50° between a side thereof and an underlying surface;

irradiating a laser light to said semiconductor island; and

reducing said crystallization promoting material existing within said semiconductor island by a second heating.

21. A method according to claim 20, wherein said first heating is performed at a temperature of 550 to 750°C.

22. A method according to claim 20, wherein said patterning is performed by an isotropic dry etching method.

23. A method according to claim 20, wherein said second heating is performed at a temperature higher than said first heating.

24. A method according to claim 22, wherein said second heating is performed in an atmosphere containing halogen gas.

25. A method according to claim 22, wherein said crystallization promoting material is selected form the group consisting of Fe, Co, Ni, Ru, Rh, Pd, OS, Ir, Pt, Cu and Au.

Abstract

Concentration of metal element which promotes crystallization of silicon and which exists within a crystalline silicon film obtained by utilizing the metal element is reduced. A first heat treatment for crystallization is performed after introducing nickel to an amorphous silicon film 103. Then, laser light is irradiated to diffuse nickel element which is concentrated locally. After that, another heat treatment is performed within an oxidizing atmosphere at a temperature higher than that of the previous heat treatment. At this time, HCl or the like is added to the atmosphere. A thermal oxide film 106 is formed in this step. At this time, gettering of the nickel element into the thermal oxide film 106 takes place. Then, the thermal oxide film 106 is removed. Thereby, a crystalline silicon film 107 having low concentration of the metal element and a high crystallinity can be obtained.

FIG.1A

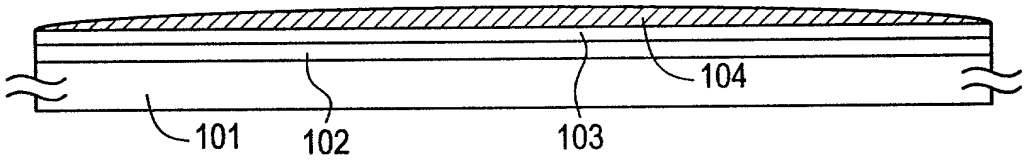


FIG.1B

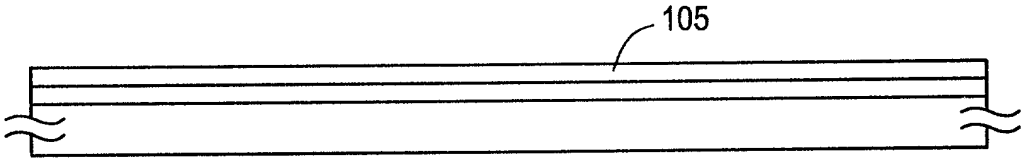


FIG.1C

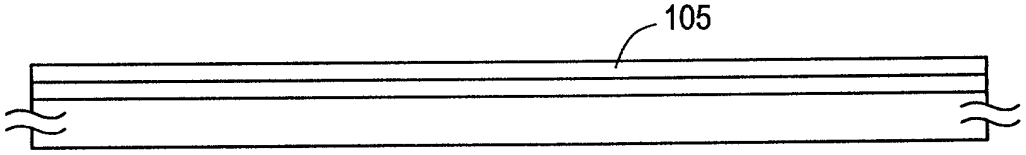


FIG.1D

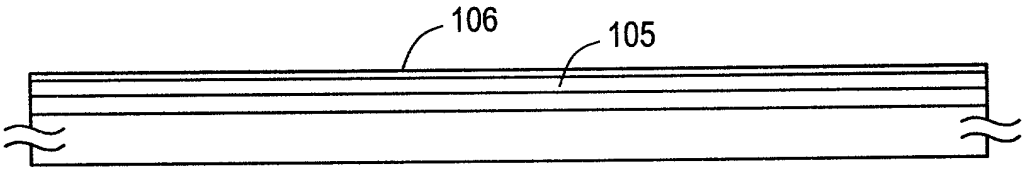


FIG.1E

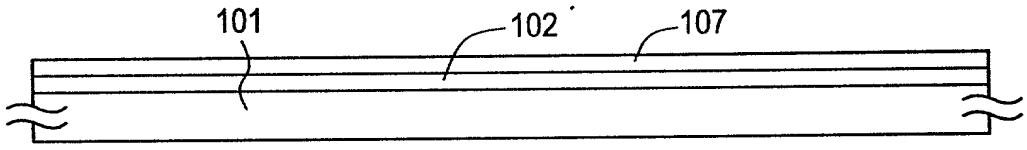


FIG.2A

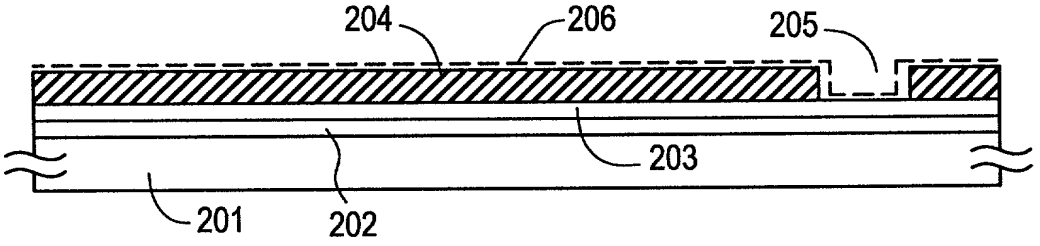


FIG.2B

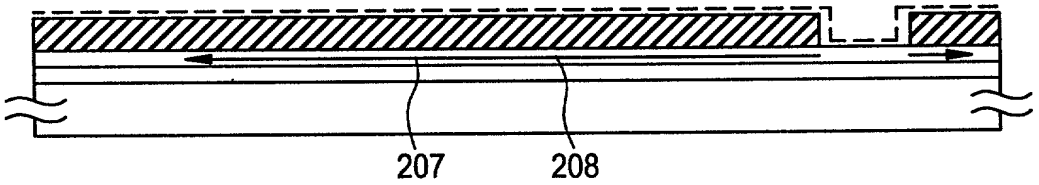


FIG.2C

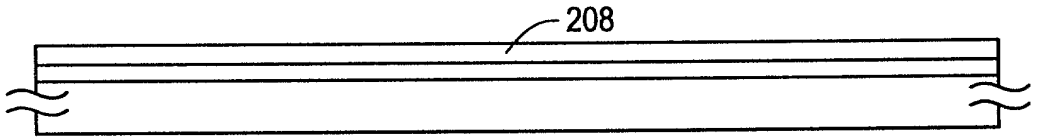


FIG.2D

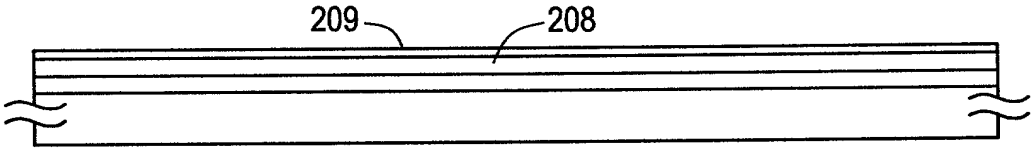


FIG.2E

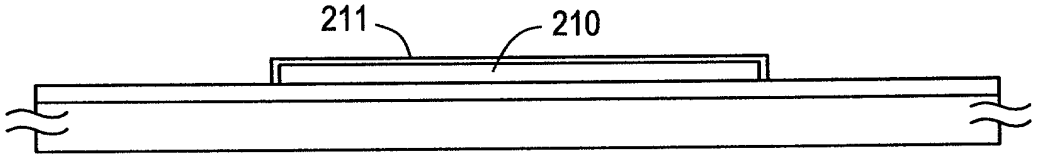


FIG.3A

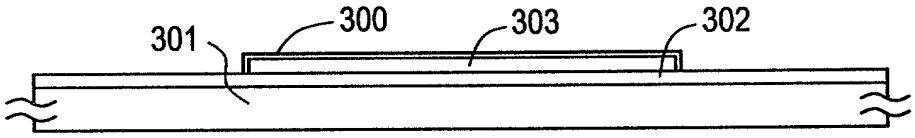


FIG.3B

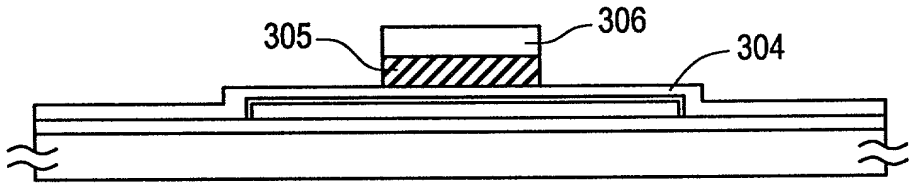


FIG.3C

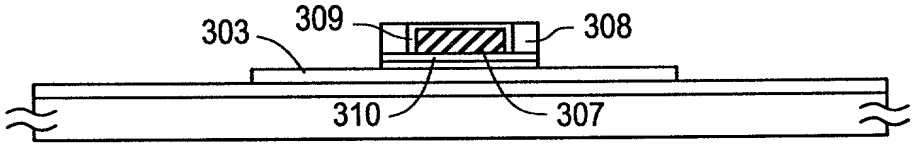


FIG.3D

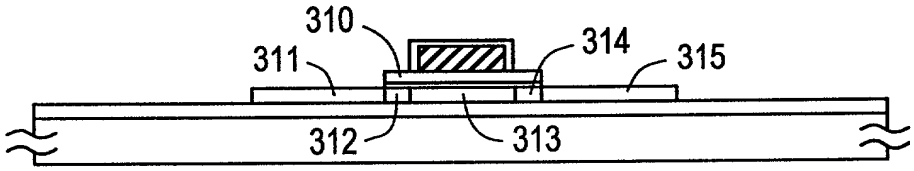


FIG.3E

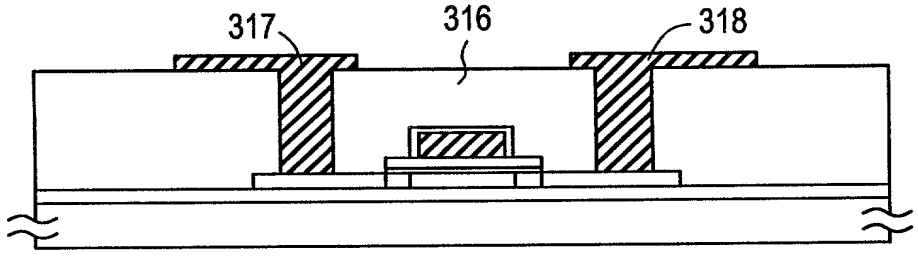


FIG.4A

FIG.4B

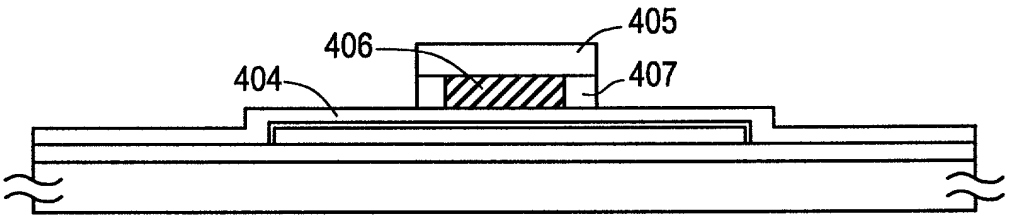


FIG.4C

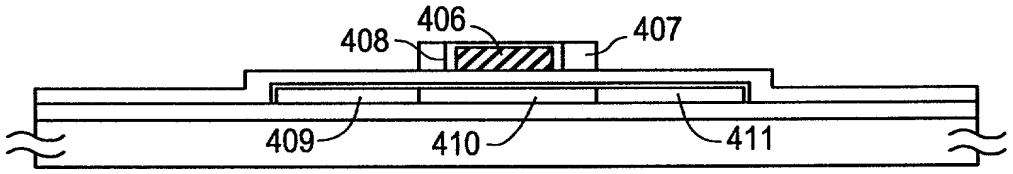


FIG.4D

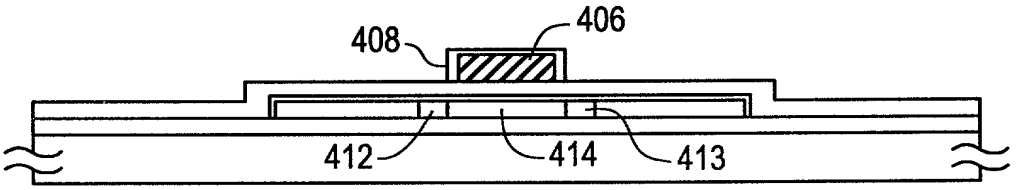


FIG.4E

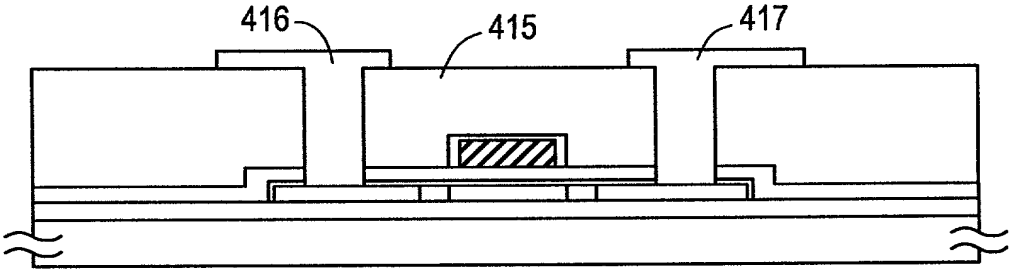


FIG.5A

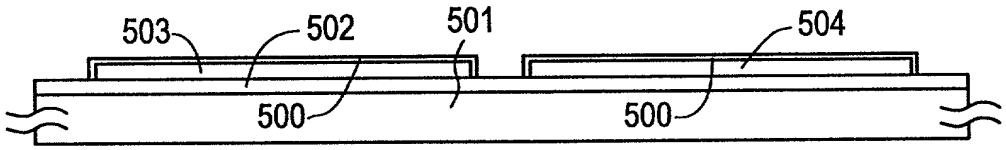


FIG.5B

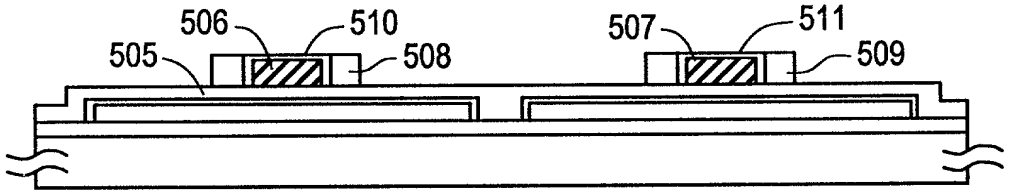


FIG.5C

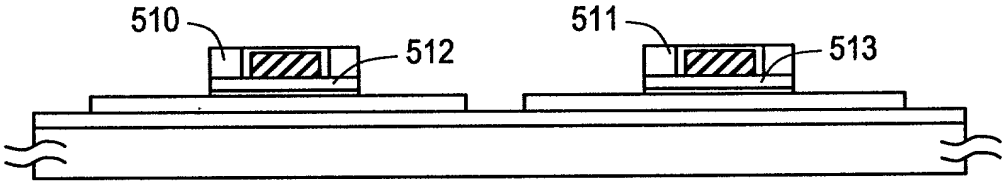


FIG.5D

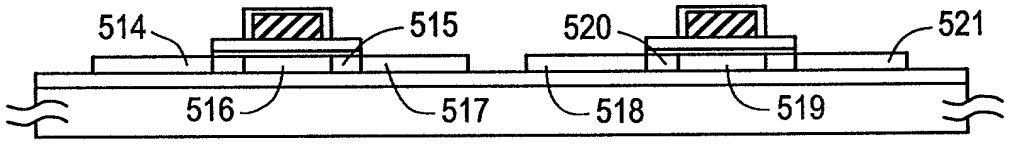


FIG.5E

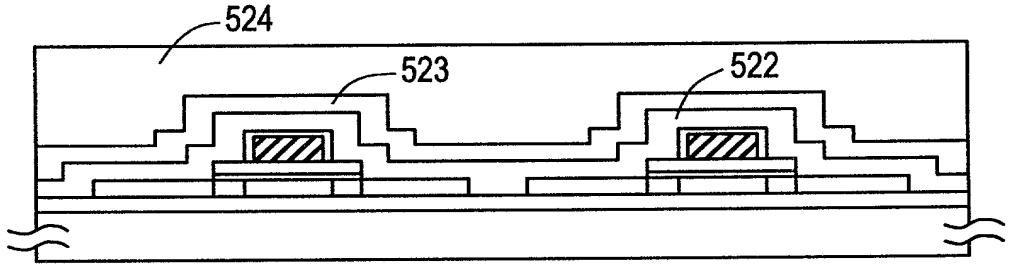


FIG.5F

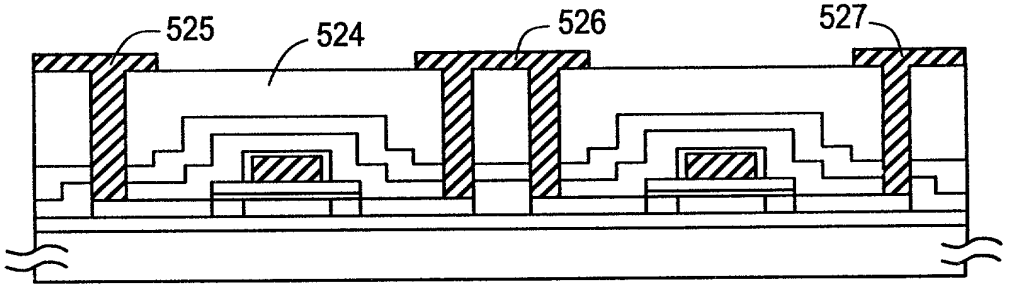


FIG.6A

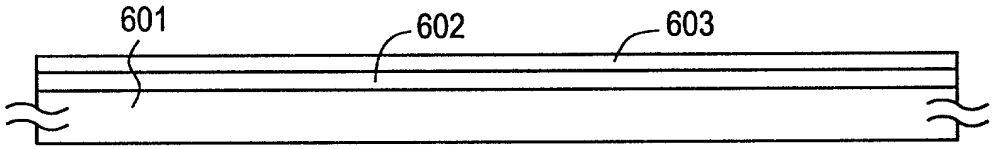


FIG.6B

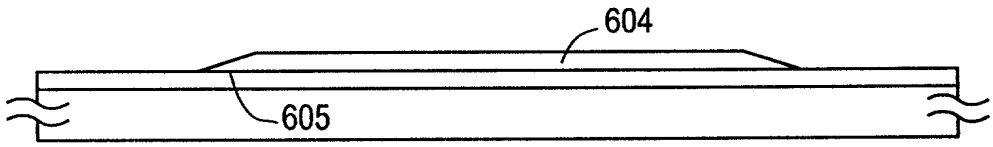


FIG.6C

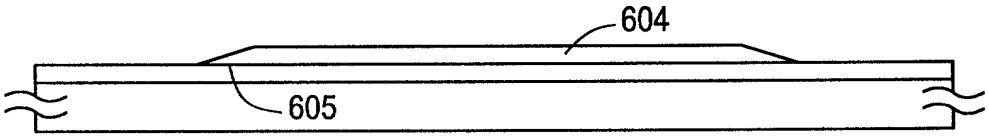


FIG.6D

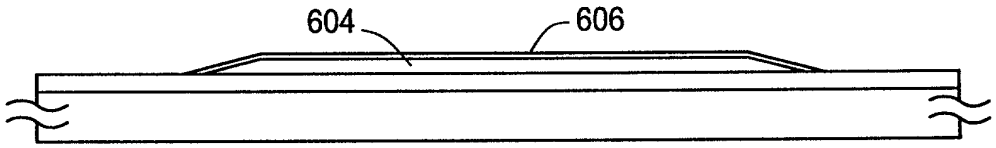


FIG.6E

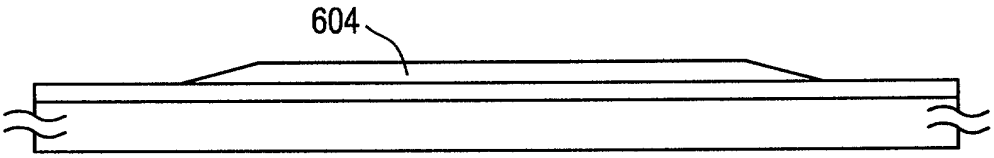


FIG.6F

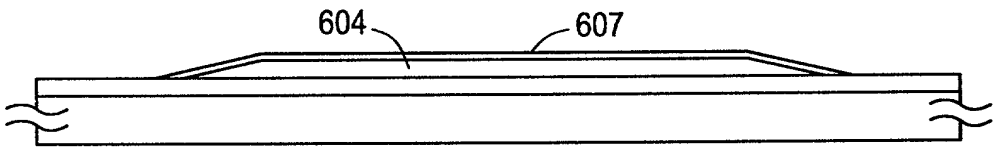


FIG.7A

IRRADIATION OF LASER LIGHT

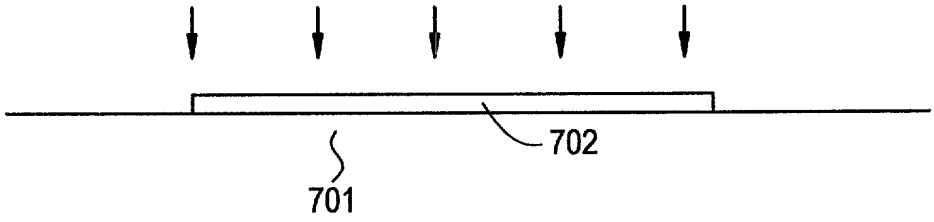
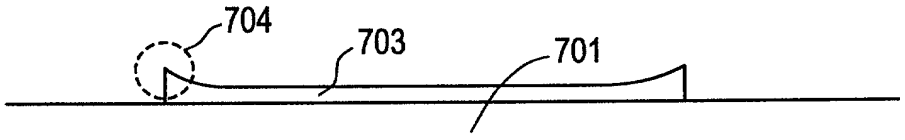


FIG.7B



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.
0756-1609

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: *

Insert Title

METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE

, the specification of which is attached hereto unless the following box is checked:

Check Box If Appropriate — For Use Without Specification Attached

☒ The specification was filed on January 16, 1997
and was assigned Serial No. 08/784,290 (if known)
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)

Priority Claimed

Insert Priority Information (if appropriate)

(Number)	(Country)	(Month/Day/Year Filed)	Yes	No
8-32874	JAPAN	January 26, 1996	☒	☐
			☐	☐
			☐	☐
			☐	☐
			☐	☐

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

Revised 11/90

*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)	Gerald J. Ferguson, Jr. (Reg. No. 23,016)
Stuart J. Friedman (Reg. No. 24,312)	David S. Safran (Reg. No. 27,997)
Charles M. Leedom, Jr. (Reg. No. 26,477)	Thomas W. Cole (Reg. No. 28,290)

Send Correspondence to:

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING ➧

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102
Telephone: (703) 790-9110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent ➧

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from _____ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of First or Sole Inventor and Date This Document Is Signed ➧

Insert Residence Insert Citizenship ➧

Insert Post Office Address ➧

FULL NAME OF SOLE OR FIRST INVENTOR	INVENTOR'S SIGNATURE		DATE
Shunpei YAMAZAKI	Shunpei Yamazaki		04/25/1997
RESIDENCE (City, State & Country)		CITIZENSHIP	
Tokyo, Japan		Japanese	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
4-10-20, Seijo, Setagaya-ku, Tokyo 157 Japan			
Second Inventor: see above — FULL NAME OF SECOND JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE		DATE
Satoshi TERAMOTO	SATOSHI TERAMOTO		05/07/1997
RESIDENCE (City, State & Country)		CITIZENSHIP	
Kanagawa, Japan		Japanese	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
Flat SEL-B 205, 304-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan			
Third Inventor: see above — FULL NAME OF THIRD JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE		DATE
Jun KOYAMA	Jun Koyama		05/07/1997
RESIDENCE (City, State & Country)		CITIZENSHIP	
Kanagawa, Japan		Japanese	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
1-4-23, Nishi-Hashimoto, Sagamihara-shi, Kanagawa-ken 229 Japan			
Fourth Inventor: see above — FULL NAME OF FOURTH JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE		DATE
Yasushi OGATA	Yasushi Ogata		05/07/1997
RESIDENCE (City, State & Country)		CITIZENSHIP	
Kanagawa, Japan		Japanese	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
Flat SEL-A 301, 304-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan			

Full Name of Fifth Inventor, if any: see above	GIVEN NAME FAMILY NAME: Masahiko HAYAKAWA	INVENTOR'S SIGNATURE: Masahiko Hayakawa	DATE: 05/07/1997
	RESIDENCE (City, State & Country): Kanagawa, Japan	CITIZENSHIP: Japanese	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country): Flat Atsugi 201, 931-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan		
Full Name of Sixth Inventor, if any: see above	GIVEN NAME FAMILY NAME: Mitsuaki OSAME	INVENTOR'S SIGNATURE: Mitsuaki OSAME	DATE: 05/07/1997
	RESIDENCE (City, State & Country): Kanagawa, Japan	CITIZENSHIP: Japanese	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country): Nurumizu Mansion 315, 1405-1, Nurumizu, Atsugi-shi, Kanagawa-ken 243 Japan		
Full Name of Seventh Inventor, if any: see above	GIVEN NAME FAMILY NAME:	INVENTOR'S SIGNATURE:	DATE:
	RESIDENCE (City, State & Country):	CITIZENSHIP:	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country):		
Full Name of Eighth Inventor, if any: see above	GIVEN NAME FAMILY NAME:	INVENTOR'S SIGNATURE:	DATE:
	RESIDENCE (City, State & Country):	CITIZENSHIP:	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country):		
Full Name of Ninth Inventor, if any: see above	GIVEN NAME FAMILY NAME:	INVENTOR'S SIGNATURE:	DATE:
	RESIDENCE (City, State & Country):	CITIZENSHIP:	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country):		
Full Name of Tenth Inventor, if any: see above	GIVEN NAME FAMILY NAME:	INVENTOR'S SIGNATURE:	DATE:
	RESIDENCE (City, State & Country):	CITIZENSHIP:	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country):		
Full Name of Eleventh Inventor, if any: see above	GIVEN NAME FAMILY NAME:	INVENTOR'S SIGNATURE:	DATE:
	RESIDENCE (City, State & Country):	CITIZENSHIP:	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country):		
Full Name of Twelfth Inventor, if any: see above	GIVEN NAME FAMILY NAME:	INVENTOR'S SIGNATURE:	DATE:
	RESIDENCE (City, State & Country):	CITIZENSHIP:	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country):		

* Note: Use this sheet for applications having more than four inventors